Course 13

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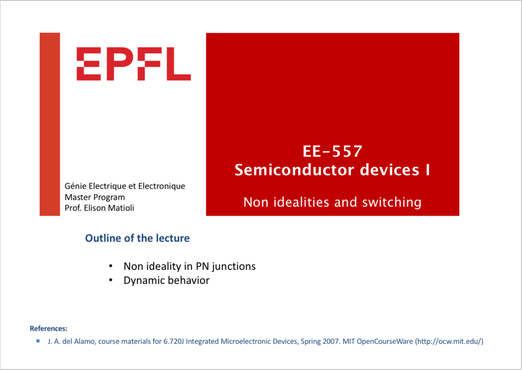
EE557 - Cours 13 -...



EPFL

Génie Electrique et Electronique
Master Program
Prof. Elison Matioli

EE-557
Semiconductor devices I

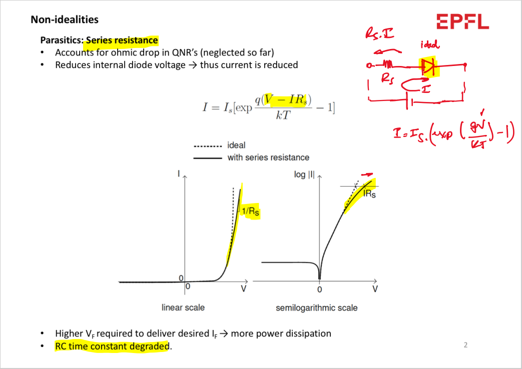
Non idealities and switching

Outline of the lecture

- Non ideality in PN junctions
- Dynamic behavior

References:

- J. A. del Alamo, course materials for 6.720J Integrated Microelectronic Devices, Spring 2007. MIT OpenCourseWare (http://ocw.mit.edu/)



Non-idealities

Parasitics: Series resistance

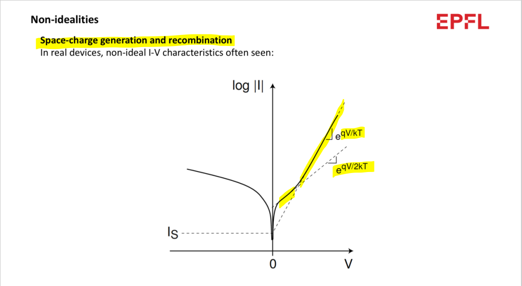
- Accounts for ohmic drop in QNR's (neglected so far)
- Reduces internal diode voltage → thus current is reduced

$$I = I_s[\exp\frac{q(V - IR_s)}{kT} - 1]$$

$R_S.I$

$I = I_S.(\exp(\frac{qV'}{kT})-1)$

- Higher V_F required to deliver desired I_F → more power dissipation
- RC time constant degraded.



Non-idealities

Space-charge generation and recombination

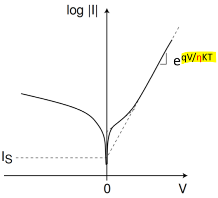
In real devices, non-ideal I-V characteristics often seen:

Anomalies often due to:

- Recombination through traps in SCR (in forward bias)
- Generation through traps in SCR (in reverse bias)

Non-idealities

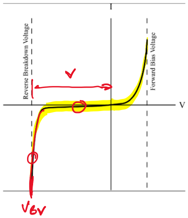
Ideality factor η

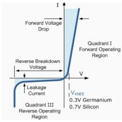


η represents the deviation from the ideal case (η = 1)

Non-idealities

Breakdown voltage



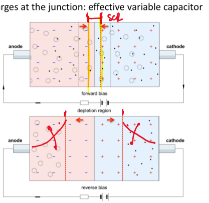


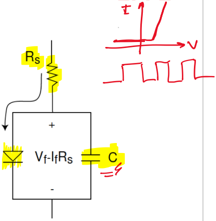
This happens when the electric field reaches the critical electric field E_{CR}

$E_{cr} = 300kV/cm$

Equivalent model of pn junctions

Charges at the junction: effective variable capacitor





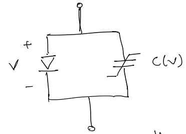
- **Depletion (junction) capacitance (C_j)**: related to the depletion at the junction
- **Diffusion capacitance (C_d)**: related to the injection of minority carriers from QNRs

Total Capacitance: Depletion (junction) capacitance (C_j) + diffusion capacitance (C_d)

$C = C_j + C_d$

$C = dQ/dV$

Equivalent model;



ideal diode with stored charges

$$I = I_s\left(\exp\frac{qV}{kT} - 1\right) + \underbrace{\frac{dQ}{dt}}_{I \propto C/s}$$

$$\frac{dQ}{dt} = \underbrace{\frac{dQ}{dV}}_{C} \cdot \frac{dV}{dt} = C \cdot \frac{dV}{dt}$$

$$I = C \cdot \frac{dV}{dt}$$

$$C = \underset{\text{diffusion}}{C_d} + \underset{\text{junction}}{C_j}$$

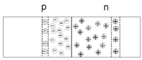
C_j : related to the change in the depletion width (SCR)

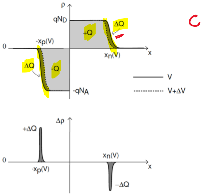
C_d : related to the amount of charges (minority carrier) that are injected in the depletion region.

Equivalent model of pn junctions

Depletion (Junction) capacitance

$C = \frac{dQ}{dV}$





$$C(V) = \frac{\epsilon}{x_{SCR}(V)}$$

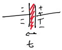
For p⁺-n junction:

$$\boxed{C(V) = \sqrt{\frac{\epsilon q N_A N_D}{2(N_D + N_A)(\phi_{bi} - V)}} = \frac{C(V=0)}{\sqrt{1 - \frac{V}{\phi_{bi}}}}}$$

$$C(V) = \sqrt{\frac{\epsilon q N_D}{2(\phi_{bi} - V)}}$$

*** Here C(V) is the capacitance per unit area, thus we must multiply by A to get the total capacitance (see class notes)

1) Junction capacitance C_j :



$$C = \varepsilon \cdot \frac{A}{t}$$

in the p-side :

$$Q_j(V) = -q \cdot N_A \cdot x_p \cdot A = -A\sqrt{\frac{2q\,\varepsilon \cdot N_D \cdot N_A \cdot (\phi_{bi} - V)}{N_D + N_A}}$$

$$Q_j(V) = Q_j(V=0) \cdot \sqrt{1 - \frac{V}{\phi_{bi}}}$$

$$C_j(V) = \frac{dQ_j(V)}{dV} = A\sqrt{\frac{q \cdot \varepsilon \cdot N_D \cdot N_A}{2(N_A + N_D) \cdot (\phi_{bi} - V)}}$$

for p⁺-n junction: $N_A \gg N_D$

$$\boxed{C_j(V) = \frac{C_j(V=0)}{\sqrt{1 - \frac{V}{\phi_{bi}}}}}$$

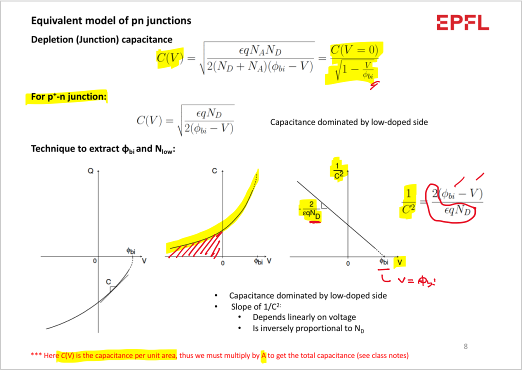
$$\Rightarrow C_j(V) = A \cdot \sqrt{\frac{q \cdot \varepsilon \cdot N_D}{2(\phi_{bi} - V)}} \Rightarrow \boxed{\frac{1}{C_j^2(V)} = \frac{2(\phi_{bi} - V)}{\varepsilon \cdot q \cdot N_D \cdot A^2}}$$

Another way of thinking :

$$C = \varepsilon \cdot \frac{A}{t} = \frac{\varepsilon \cdot A}{x_{scr}}$$

$$C = \frac{\varepsilon \cdot A}{x_{scr}} = \frac{\varepsilon A}{\sqrt{\frac{2\varepsilon(N_D+N_A)}{q \cdot N_A \cdot N_D}\cdot(\phi_{bi}-V)}}$$

$$C = \sqrt{\frac{\varepsilon \cdot q \cdot N_A \cdot N_D}{2(N_D+N_A)\cdot(\phi_{bi}-V)}} \cdot A$$



Equivalent model of pn junctions

Depletion (Junction) capacitance

$$C(V) = \sqrt{\frac{\epsilon q N_A N_D}{2(N_D+N_A)(\phi_{bi}-V)}} = \frac{C(V=0)}{\sqrt{1-\frac{V}{\phi_{bi}}}}$$

For p^+-n junction:

$$C(V) = \sqrt{\frac{\epsilon q N_D}{2(\phi_{bi}-V)}}$$

Capacitance dominated by low-doped side

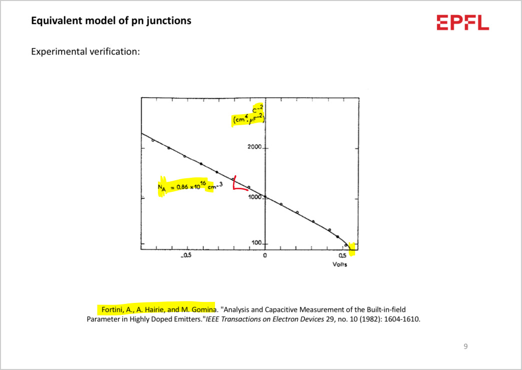
Technique to extract ϕ_{bi} and N_{low}:

Q
0
φbi
V
C
C
0
φbi
V
$\frac{1}{C^2}$
$-\frac{2}{\epsilon q N_D}$
0
φbi
V
V = φbi

$$\frac{1}{C^2} = \frac{2(\phi_{bi}-V)}{\epsilon q N_D}$$

- Capacitance dominated by low-doped side
- Slope of $1/C^2$:
  - Depends linearly on voltage
  - Is inversely proportional to N_D

*** Here C(V) is the capacitance per unit area, thus we must multiply by A to get the total capacitance (see class notes)



Equivalent model of pn junctions

Experimental verification:

C^{-2}
$(cm^4 \cdot pF^{-2})$
2000
1000
100
$N_A = 0.86 \times 10^{16}\ cm^{-3}$
-0.5
0
0.5
Volts

Fortini, A., A. Hairie, and M. Gomina. "Analysis and Capacitive Measurement of the Built-in-field Parameter in Highly Doped Emitters."*IEEE Transactions on Electron Devices* 29, no. 10 (1982): 1604-1610.

Equivalent model of pn junctions

Exercise:

Consider a p-n junction with $N_A=5\times10^{18}$ cm^{-3} and $N_D = 10^{17}$ cm^{-3}. The diode has an area of 10 um^2. Estimate the junction capacitance associated with this diode at room temperature and under an applied bias of 0.6 V.

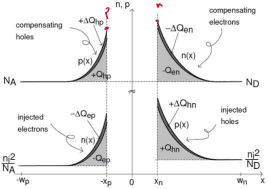
$$C_j = \sqrt{\frac{\varepsilon \cdot q \cdot N_A \cdot N_D}{2(N_D+N_A)\cdot(\Phi_{bi}-V)}} \cdot A$$

- $x_{sce} = 110nm$ (for $V=0$) $= 0.11\ \mu m$
- $C_j(V=0) = A \cdot \frac{\varepsilon}{x_{sce}(V=0)} = 10 \times 10^{-8}\ cm^2 \cdot \frac{11.7 \cdot 8.85\times10^{-14}\ F/cm}{0.11 \times 10^{-4}\ cm} = \boxed{1.0\ fF}$
- $C_j(V) = \frac{C_j(V=0)}{\sqrt{1-\frac{V}{\Phi_{bi}}}} = \frac{1\ fF}{\sqrt{1-\frac{V}{0.94}}} \overset{V=0.6}{=} \boxed{1.66\ fF}$

Equivalent model of pn junctions

Diffusion capacitance: **due to minority carrier storage**

Quasi-neutrality in QNR's demands n' ~ p' :



majority

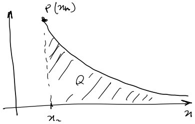
minority

In n-QNR, quasi-neutrality implies: $Q_{hn} \simeq |Q_{en}| \equiv Q_n$

Also, if $V \uparrow \rightarrow Q_{hn} \uparrow \rightarrow |Q_{en}| \uparrow$ with:

$$\Delta Q_{hn} \simeq |\Delta Q_{en}| \equiv \Delta Q_n$$

ΔQ_{hn} supplied from p-contact, ΔQ_{en} supplied from n-contact



$$p'(x) = p'(x_n) \cdot \exp\left(-\frac{x-x_n}{L_h}\right)$$

to calculate charges Q, integrate this expression:

$$Q_h = \int_{x_n}^{\infty} p'(x) \cdot A \cdot q\ dx$$

$[cm^{-3}]\ cm^2 \cdot C \cdot cm$

#1 $\{ Q_n = q \cdot A \cdot p'(x_n) \cdot L_h$ [1]

#2 $\left\{ \begin{array}{l} J_e = -q \cdot n' \cdot v_e^{diff} \longrightarrow n' = \frac{J_e}{q \cdot v_e} \\ v_e^{diff} = -\frac{D_e}{L_e} \quad \begin{array}{l}[cm^2/s] \\ [cm]\end{array} \end{array} \right.$

Using (1) and (2):

$$\begin{cases} Q_p = q \cdot A \cdot L_e \cdot n'(-x_p) = \overset{cm^2}{A} \cdot \frac{L_e^2}{D_e} \cdot \overset{[A/cm^2]}{J_e(-x_p)} = \frac{L_e^2}{D_e} \cdot I_e(-x_p) \\ Q_n = q \cdot A \cdot L_h \cdot p'(+x_n) = A \cdot \frac{L_h^2}{D_h} \cdot J_h(+x_n) = \frac{L_h^2}{D_h} \cdot I_h(+x_n) \end{cases}$$

Also:

lifetime of minority carriers

$$\begin{cases} Q_p = \tau_e \times I_e \\ Q_n = \tau_h \times I_h \end{cases}$$

$$\tau_e = \frac{L_e^2}{D_e}$$

Diffusion length

Diffusion coefficient

$$Q_d = Q_p + Q_n = \tau_e I_e + \tau_h I_h = Q_s \cdot \left(\exp \frac{qV}{kT} - 1\right)$$

we would like to calculate C_d:

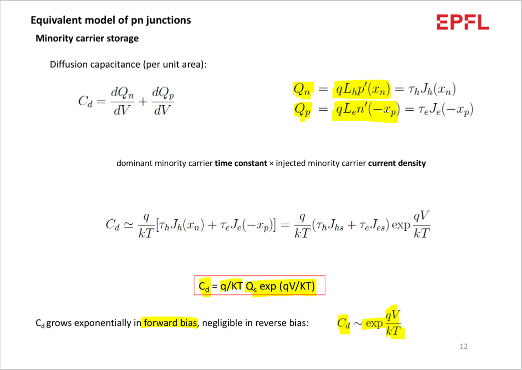
$$\boxed{C_d = \frac{dQ_d}{dV} = \frac{q}{kT} \cdot \exp\left(\frac{qV}{kT}\right)}$$

if $V \gg kT$

$$\boxed{C_d \simeq \frac{q}{kT} \cdot Q_d}$$

Total capacitance:

$$\boxed{C = C_d + C_j}$$



Equivalent model of pn junctions

Minority carrier storage

EPFL

Diffusion capacitance (per unit area):

$$C_d = \frac{dQ_n}{dV} + \frac{dQ_p}{dV}$$

$$Q_n = qL_h p'(x_n) = \tau_h J_h(x_n)$$
$$Q_p = qL_e n'(-x_p) = \tau_e J_e(-x_p)$$

dominant minority carrier **time constant** × injected minority carrier **current density**

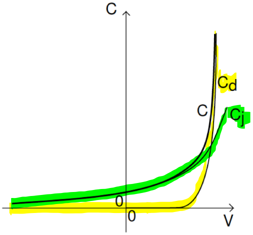
$$C_d \simeq \frac{q}{kT}[\tau_h J_h(x_n) + \tau_e J_e(-x_p)] = \frac{q}{kT}(\tau_h J_{hs} + \tau_e J_{es}) \exp\frac{qV}{kT}$$

$C_d = q/KT\ Q_s \exp(qV/KT)$

C_d grows exponentially in forward bias, negligible in reverse bias: $C_d \sim \exp\frac{qV}{kT}$

Equivalent model of pn junctions

Total diode capacitance:



Junction capacitance:
Dominant at negative V

$$C(V) = \sqrt{\frac{\epsilon q N_D}{2(\phi_{bi} - V)}}$$

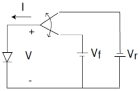
Diffusion capacitance:
Dominant at positive bias

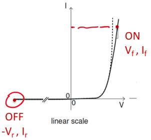
$$C_d \sim \exp\frac{qV}{kT}$$

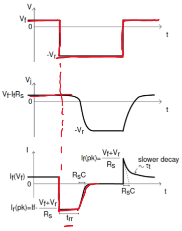
Dynamics: Switching behavior of pn diodes

Fundamental weakness of p-n diodes: **minority carrier storage slows down p-n diode**

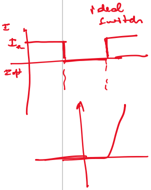
Consider simple voltage switching:







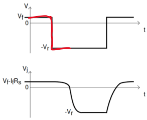
Delays are associated with R_sC_j and with minority carrier storage.

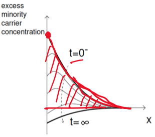


Dynamics: Switching behavior of pn diodes

Switch-off transient

Evolution of excess minority carrier concentration:





switch-off

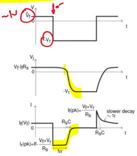
At t =0⁻, $V_f \rightarrow I_f$; minority carrier stored charge: $Q = \tau_t I_f$

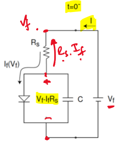
with τ_t: dominant minority carrier time constant.

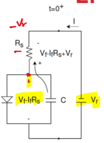
At t =0⁺, external V abruptly changes from V_f to $-V_r$; internal V cannot change abruptly
→ need to get rid of minority carriers!

Dynamics: Switching behavior of pn diodes

Switch-off transient







$$I(0^-) = I_f(V_f)$$

$$I(0^+) = -\frac{1}{R_s}(\underbrace{V_f - I_f R_s + V_r}_{V_f - I_f \cdot R_s - (-V_r)}) \simeq \boxed{-\frac{V_r}{R_s}}$$

$|V_r| \gg V_f$

Two phases to discharge:

Phase I - From $V_j = V_f - I_f R_s$ to $V_j \approx 0$.

Since $Q \sim \exp(qV_f/KT)$, as Q discharges, V_f cannot change much.

Discharge proceeds nearly at constant current $I_r(pk) \sim -V_r/R_s$: limited by R_s

Time to discharge (**reverse recovery time**):

$$t_{rr} \simeq \frac{Q}{|I_r(pk)|} \simeq \overset{Q}{\tau_t I_f(V_f)} \underset{I_r}{\frac{R_s}{V_r}}$$

$V_f \ll |V_r|$: $t_{rr} \ll \tau$ removing carriers is much faster than letting them recombine!

Phase II - From $V_j \sim 0$ to $V_j = -V_r$.

Discharge of the depletion capacitance → R_sC_j time constant is what limits this process

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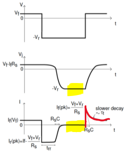
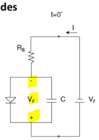
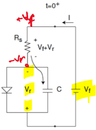
Dynamics: Switching behavior of pn diodes

Switch-on transient







$$I(0^+) = \frac{V_f + V_r}{R_s}$$

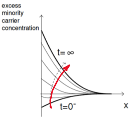
produces a peak of current

$$I(0^-) = -I_s$$

$$I(0^+) = \frac{V_f + V_r}{R_s}$$

Evolution of excess minority carrier concentration:

- First, R_sC_j-type charge up of junction capacitance: V_j increases
- Then, minority carrier charge injection → takes τ_t
  (τ is the dominant minority carrier time constant)
- After a few τ_t the system reaches equilibrium



switch-on

Equivalent model of pn junctions

Exercise:

Consider a p-n junction with N_A=5x10^{18} cm^{-3} and N_D = 1x10^{17} cm^{-3}. The diode has an area of 10 um^2 and the p and n regions are long (>> L) Estimate the diffusion capacitance associated with this diode at room temperature and under an applied bias of 0.6 V.

Key conclusions

Junction or depletion capacitance:
Depletion capacitance due to SCR width modulation:

$$C(V) = \frac{\epsilon}{x_{SCR}(V)}$$

Diffusion capacitance arises from minority carrier storage in QNR's and quasi-neutrality:

$$C_d = \frac{q}{kT}\Sigma_{n,p}$$

(dominant minority carrier time constant × minority carrier current density)

$$C_d \propto J \propto \exp\frac{qV}{kT} \Rightarrow C_d$$

C_d dominates in forward bias, C_j dominates in reverse bias.

Dynamics of p-n diode **dominated by minority carrier storage**.

Reverse recovery time is **time required to eliminate minority carrier** stored charge in switch-off transient.